Amend paragraph 15 to read as follows:

A2

FIG. 2 is a schematic diagram of a typical one of the clock receivers shown in FIG. 1; and

Add the following paragraph after paragraph 15:

A3

FIG. 3 is a waveform diagram that illustrates a differential sinusoidal signal pair that may be generated in the clock signal generation and distribution arrangement of FIG. 1.

Amend paragraph 18 to read as follows:

A4

In FIG. 1, reference numeral 10 indicates a signal generator which generates a differential sinusoidal signal pair. As is well understood by those who are skilled in the art, a differential sinusoidal signal pair comprises a pair of sinusoidal wave forms, that are substantially equal in frequency and amplitude but that are substantially 180° out of phase with each other, as illustrated in FIG. 3. The differential sinusoidal signal pair generated by signal generator 10 may, for example, have a peak to peak differential (ppD) of about 100 mV or 150 mV. The common mode level of the differential sinusoidal signal pair may be at the center of the power supply voltage. For example, each signal of the pair may swing from about 575 mV to 625 mV when a 1.2 volt power supply is used. It will be recognized that such a differential sinusoidal signal pair has a peak to peak differential of 100 mV. It is contemplated to employ a differential sinusoidal signal pair having a different common mode and/or a different peak to peak differential than the signals which have been described above.

Amend paragraph 23 to read as follows:

It may be desirable for the distribution circuitry 12 to be routed and loaded so as to have inductance and capacitance that produces resonance at the desired frequency of operation. This further reduces the clock power requirements. Switchable loads 14 may be included in the distribution circuitry 12 to permit the load of the distribution circuitry 12 to be tuned to compensate for manufacturing variations.

In the Claims:

Amend claim 13 to read as follows:

13. (Amended) A clock circuit for an IC, comprising:

a generating circuit adapted to generate a differential sinusoidal signal pair;

a distribution circuit coupled to the generating circuit and adapted to distribute the differential sinusoidal signal pair on the IC; and

a plurality of clock receiver circuits coupled to the distribution circuit and adapted to convert the differential sinusoidal signal pair into respective local clock signals.

REMARKS

Claims 1-30 remain in this application. The pending claims stand rejected and are now presented for reconsideration in view of the following remarks.